

Abstract of the Disclosure:

A vertical semiconductor transistor component is built up on a substrate by using a statistical mask. The vertical semiconductor transistor component has vertical pillar structures statistically distributed over the substrate. The vertical pillar structures are electrically connected on a base side thereof to a first common electrical contact. The vertical pillar structures include, along the vertical direction, layer zones of differing conductivity, and have insulation layers on their circumferential walls. An electrically conductive material is deposited between the pillar structures and forms a second electrical contact of the semiconductor transistor component. The pillar structures are electrically contacted to a third common electrical contact on their capping side.

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